Spec

asynchronous clock rate FIFO

EVENT EDGE SYNCHRONIZATION SYSTEM AND METHOD OF OPERATION THEREOF

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention is directed, in general, to a communications system and, more specifically, to an event edge synchronization system and method of operating the same.

BACKGROUND OF THE INVENTION

[0002] Communications networks are currently undergoing a revolution brought about by the increasing demand for real-time information being delivered to a diversity of locations. Many situations require the ability to transfer large amounts of data across geographical boundaries with increasing speed and accuracy. However, with the increasing size and complexity of the data that is currently being transferred, maintaining the speed and accuracy is becoming increasingly difficult.

[0003] Early communications networks resembled a hierarchical star topology. All access from remote sites was channeled back to a central location where a mainframe computer resided. Thus, each transfer of data from one remote site to another, or from one remote site to the central location, had to be processed by the

central location. This architecture is very processor-intensive and incurs higher bandwidth utilization for each transfer. This was not a major problem in the mid to late 1980s where fewer remote sites were coupled to the central location. Additionally, many of the remote sites were located in close proximity to the central location. Currently, hundreds of thousands of remote sites are positioned in various locations across assorted continents. Legacy networks of the past are currently unable to provide the data transfer speed and accuracy demanded in the marketplace of today.

[0004] In response to this exploding demand, data transfer through networks employing distributed processing has allowed larger packets of information to be accurately and quickly distributed across multiple geographic boundaries. Today, many communication sites have the intelligence and capability to communicate with many other sites, regardless of their location. This is typically accomplished on a peer level, rather than through a centralized topology, although a host computer at the central site can be appraised of what transactions take place and can maintain a database from which management reports are generated and operation issues addressed.

[0005] Distributed processing currently allows the centralized site to be relieved of many of the processor-intensive data transfer requirements of the past. This is typically accomplished using a data network, which includes a collection of routers. The

routers allow intelligent passing of information and data files between remote sites. However, increased demand and the sophistication required to route current information and data files quickly challenged the capabilities of existing routers. Also, the size of the data being transmitted is dramatically increasing. Some efficiencies are obtained by splitting longer data files into a collection of smaller, somewhat standardized cells for transmission or routing. However, these efficiencies are somewhat offset by the processing required to process the cells at nodes within the network.

[0006] More specifically, within the system there are limitations associated with passing event signals between two different subsystems or within a subsystem that employs two clock zones having asynchronous clock rates. Currently, this typically requires a "four-edge" synchronization process between the two asynchronous clock zones. This four-edge synchronization process requires the generation of a first event signal in a first clock zone that is then recognized and acknowledged by a first event signal in the second clock zone. A second event signal is then generated in the first clock zone to acknowledge that the second clock zone has acknowledged the first event signal in the first clock zone. Then, a second event signal is generated in the second clock zone that acknowledges the second event signal acknowledgment in the first clock zone. This process is time consuming and slows

the interchange of information or data within a system or subsystem.

[0007] Accordingly, what is needed in the art is an enhanced way to pass event signals between two asynchronous clock zones.

SUMMARY OF THE INVENTION

[0008] To address the above-discussed deficiencies of the prior art, the present invention provides an event edge synchronization system and a method of operating the same. In one embodiment, the event edge synchronization system includes: (1) a first clock zone device configured to generate an event signal based upon a first clock rate, (2) a second clock zone device configured to operate at a second clock rate, which is asynchronous with the first clock rate and (3) a synchronous notification subsystem configured to receive the event signal, synchronize the event signal to the second clock rate based upon an edge transition of the event signal and the second clock rate, and generate a synchronous notification signal therefrom.

[0009] In another embodiment, the present invention provides a method of operating an event edge synchronization system that includes: (1) generating an event signal based upon a first clock rate associated with a first clock zone device, (2) operating a second clock zone device at a second clock rate, which is asynchronous with the first clock rate, (3) receiving the event signal, (4) synchronizing the event signal to the second clock rate based upon an edge transition of the event signal and the second clock rate, and (5) generating a synchronous notification signal therefrom.

[0010] In another embodiment, the present invention also provides an event edge synchronization system that includes: (1) a first clock zone device means that generates an event signal based upon a first clock rate, (2) a second clock zone device means that operates at a second clock rate, which is asynchronous with the first clock rate and (3) a synchronous notification subsystem means that receives the event signal, synchronizes the event signal to the second clock rate based upon an edge transition of the event signal and the second clock rate, and generates a synchronous notification signal.

[0011] The present invention also provides, in another embodiment, a fast pattern processor that includes: (1) a data buffer that stores processing blocks associated with a protocol data unit (PDU), (2) a context memory subsystem associated with the data buffer that receives the processing blocks, (3) a pattern processing engine, associated with the context memory, that performs pattern matching upon the processing blocks and (4) an output interface subsystem that receives the processing blocks from the data buffer or the context memory subsystem and re-transmits packets or payloads embodied within the processing blocks.

[0012] The output interface subsystem further including a first-in-first-out (FIFO) buffer and an event edge synchronization system that provides a synchronous notification signal indicating that a

block of data of the FIFO buffer has been retrieved and re-transmitted. The event edge synchronization system includes: (1) a first clock zone device that generates an event signal based upon a first clock rate, the first clock zone device is associated with an output portion of the FIFO buffer, (2) a second clock zone device that receives the synchronous notification signal based upon a second clock rate and performs processing based upon the synchronous notification signal, the second clock rate asynchronous with the first clock rate and (3) a synchronous notification subsystem that receives the event signal, synchronizes the event signal to the second clock rate based upon an edge transition of the event signal and the second clock rate, and generates the synchronous notification signal.

[0013] The foregoing has outlined, rather broadly, preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its

broadest form.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0015] FIGURE 1 illustrates a block diagram of an embodiment of a communications network, constructed in accordance with the principles of the present invention;

[0016] FIGURE 2 illustrates a block diagram of an embodiment of a router architecture, constructed in accordance with the principles of the present invention;

[0017] FIGURE 3 illustrates a block diagram of an embodiment of a fast pattern processor (FPP), constructed in accordance with the principles of the present invention;

[0018] FIGURE 4 illustrates a block diagram of an embodiment of a output interface subsystem, constructed in accordance with the principles of the present invention;

[0019] FIGURE 5 illustrates a block diagram of an embodiment of a synchronous notification subsystem, constructed in accordance with the principles of the present invention;

[0020] FIGURE 6 illustrates a logic diagram of an embodiment of a synchronous notification subsystem, constructed in accordance with the principles of the present invention; and

[0021] FIGURE 7 illustrates a timing diagram showing timing events associated with an embodiment of a synchronous notification signal constructed in accordance with the principles of the present invention.

DETAILED DESCRIPTION

[0022] Referring initially to FIGURE 1, illustrated is a block diagram of an embodiment of a communications network, generally designated 100, constructed in accordance with the principles of the present invention. The communications network 100 is generally designed to transmit information in the form of a data packet from one point in the network to another point in the network.

[0023] As illustrated, the communications network 100 includes a packet network 110, a public switched telephone network (PSTN) 115, a source device 120 and a destination device 130. In the illustrative embodiment shown in FIGURE 1, the packet network 110 comprises an Asynchronous Transfer Mode (ATM) network. However, one skilled in the art readily understands that the present invention may use any type of packet network. The packet network 110 includes routers 140, 145, 150, 160, 165, 170 and a gateway 155. One skilled in the pertinent art understands that the packet network 110 may include any number of routers and gateways.

[0024] The source device 120 may generate a data packet to be sent to the destination device 130 through the packet network 110. In the illustrated example, the source device 120 initially sends the data packet to the first router 140. The first router 140 then determines from the data packet which router to send the data packet to based upon routing information and network loading. Some

[0042] Additionally, coupled to the internal function bus 310 is an output interface 306. The output interface 306 sends PDUs and their classification conclusions to the downstream logic. The output interface 306 may retrieve the processing blocks stored in the data buffer 340 and send the PDUs embodied within the processing blocks to an external unit through an output data port 338. The output data port 338, in an exemplary embodiment, is a 32-bit POS-PHY connected to the RSP 230 (FIGURE 2).

[0043] Turning now to FIGURE 4, illustrated is a block diagram of an embodiment of a output interface subsystem, generally designated 400, constructed in accordance with the principles of the present invention. The output interface subsystem 400 may be embodied in a fast pattern processor (FPP), as described in FIGURE 3 above. The output interface subsystem 400 receives processing blocks, associated with a protocol data unit (PDU), from a data buffer or a context memory subsystem within the FPP and re-transmits packets or payloads embodied within the processing blocks to an output port 412. The data buffer and context memory subsystem are discussed in more detail in FIGURE 3.

[0044] The output interface subsystem 400 includes a first-in-first-out (FIFO) buffer 410, an event edge synchronization system 420 and a controller 430. The FIFO buffer 410 provides a buffering function by accepting processing blocks at its input 411 and clocking them through a collection of storage positions until they

are transmitted via the output port 412. The FIFO buffer 410 employs a first clock zone having a first clock rate CR1 that is associated with clocking the processing blocks through an output portion of the FIFO buffer 410.

[0045] Additionally, the FIFO buffer 410 employs a second clock zone having a second clock rate CR2 that is associated with clocking the processing blocks through an input portion of the FIFO buffer 410. The first and second clock zones allow the FIFO buffer 410 to accommodate different timing requirements for processing blocks being retrieved and re-transmitted by the output interface subsystem 400. The first and second clock rates CR1, CR2, are asynchronous, meaning that the clocking transitions associated with the first and second clock rates CR1, CR2, do not always occur at the same time.

[0046] In the illustrated embodiment, the event edge synchronization system 420 provides a synchronous notification signal indicating that a block of data of the FIFO buffer 410 has been retrieved and re-transmitted. The event edge synchronization system 420 includes a first clock zone device 422, a second clock zone device 424 and a synchronous notification subsystem 426 The first clock zone device 422 is associated with the first clock zone of the FIFO buffer 410 and generates an event signal based upon the first clock rate CR1. This event signal is provided to the synchronous notification subsystem 426.

[0047] The synchronous notification subsystem 426 receives the event signal and synchronizes this event signal to the second clock rate CR2 provided by the second clock zone device 424, which is associated with the second clock zone of the FIFO buffer 410. This synchronization is based upon an edge transition of the event signal and the second clock rate CR2. The synchronous notification subsystem 426 generates the synchronous notification signal based upon this synchronization. The second clock zone device 424 receives the synchronous notification signal, further performs processing based upon it and provides synchronization information to the controller 430. The controller 430 uses the synchronization information provided to orchestrate the operation of the FIFO buffer 410, in the illustrated embodiment. Additionally, the controller 430 may also use the synchronization information to send a control or an acknowledgment signal to a device external to the output interface subsystem 400.

[0048] In another embodiment of the present invention, a second event edge synchronization system may also be employed to create a second synchronous notification signal that may be used for acknowledgment or handshaking between the first and second clock zones. For example, the controller 430 may send an acknowledgment event to the first clock zone device of the second event edge synchronization system in response to the synchronous notification signal generated by the first event edge synchronization system